REVISED TENTATIVE COURSE SCHEDULE

Date	**Topic(s)**	**Reading**	**Written Work Due**
		(All in main text by Harris unless otherwise stated)	
W 8/28	Course Introduction; The Levels of Computer Structure; Architecture and Organization		
F 8/30	Levels, etc. (continued)	§1.1-1.3	
M 9/2	*Labor Day - no class*		
T 9/3	Lab: Levels of Computer Structure (1) KOSC 241		
W 9/4	Introduction to Digital Logic: Combinatorial Logic	§1.5, 2.1, 2.3-2.4	**LAB 1 DUE**
F 9/6	(continued)	§2.2, 2.5-2.7	
M 9/9	(continued)	§1.6-1.9 (1.7 optional); §2.8-2.10, §5.1-5.2 through top of p. 241	
T 9/10	Lab: Realizing Boolean expressions with TTL SSI gates (2) KOSC 241		
W 9/11	Sequential Logic	§3.1-3.2	**LAB 2 DUE**
F 9/13	(continued)	§3.3-3.5	
M 9/16	(continued)	§3.6-3.7	
T 9/17	Lab: Sequential Circuits (3) KOSC 244		
W 9/18	Guest Speaker		**(One writeup due next week for Labs 3 and 4)**
F 9/20	Representing Information in Binary	§1.4	
M 9/23	(continued)	§5.3.2	**START BINARY DRILLS**
T 9/24	Lab: Sequential Circuits ctd (4) KOSC 241		
W 9/25	Error Detecting and Correcting Codes		**LABS 3-4 DUE**
F 9/27	Introduction to the MIPS Architecture and Assembly Language	§6.1-6.4.1; §6.7.3; MIPS ISA Handout	
M 9/30	(continued)	§6.4.2, 6.4.5	
T 10/1	Lab: MIPS Machine and Assembly Language (5) KOSC 244		

W 10/2	Control Structures; MIPS Branch and Jump Instructions	§6.4.3-6.4.4; Control Structures Handout	**LAB 5 DUE**
F 10/4	(continued)		
M 10/7	Procedures and Parameter Passing	§6.4.6; MIPS Procedures Handout	
T 10/8	Lab: Using the MIPS Assembler and Debugger (6) KOSC 244		
W 10/9	Procedures and Parameter Passing (continued)	§6.6	**LAB 6 DUE**
F 10/11	Exceptions and Interrupts	§6.7.2; Exception-Handling Handout	
M 10/14	Other CPU Architectures: 0, 1, 2 and 3 address machines; addressing modes; CISC's vs RISC's	§6.5, 6.8-6.9	
T 10/15	Lab: Data Structures and Addressing Memory (7) KOSC 244		
W 10/16	Review and Catch Up		**LAB 7 DUE**
F 10/18	*No class - quad break*. Binary Drills due by 4 PM **Thursday**		**BINARY DRILLS DUE BY 4:00 THURSDAY**
M 10/21	Other CPU Architectures (continued)		**TAKE-HOME MIDTERM EXAM (THROUGH EXCEPTIONS AND INTERRUPTS) DUE**
T 10/22	Lab: Procedures; Recursion (8) KOSC 244		
W 10/23	CPU Implementation; The Register Transfer Level; Internal Busses and the ALU	§5.2 (omit 5.2.6 -5.2.7) §7.1	**LAB 8 DUE**
F 10/25	(continued)	§7.3-7.4	
M 10/28	Control Unit Implementation: Hardwired and Microprogrammed Control		
T 10/29	Lab: Data Paths and MUXes (9) KOSC 244		
W 10/30	Pipelining; Superscalar Computers; Instruction-Level Parallelism	§3.6, 7.5	**LAB 9 DUE**
F 11/1	(continued)	§7.8	
M 11/4	Memory Devices	§5.5,2-5.5.4	

T 11/5	*Day of Prayer - No Lab*		
W 11/6	Memory Devices(continued)	§5.5.6	
F 11/8	(continued)	§5.5.1	
M 11/11	Memory Hierarchies	§8.1-8.3	
T 11/12	Lab: Control Units (10) KOSC 244		
W 11/13	Memory Hierarchies (continued)		**LAB 10 DUE**
F 11/15	Memory Hierarchies (continued)	§8.4, §8.8-8.9	
M 11/18	(continued)		
T 11/19	Lab: Memory Devices (11) KOSC 241		
W 11/20	The Input-Output Subsystem; Bus Structures; Inerrupts and DMA	§8.5 quickly skim; §8.6-8.7	**LAB 11 DUE**
F 11/22	IO (continued)		
M 11/25	(continued)	§8.5, quickly skim §8.6-§8.7	
T 11/26	Lab: TBA		
W 11/27	*Thanksgiving Break - no class*		
R 11/28	*Thanksgiving Break - no lab*		
F 11/29	*Thanksgiving Break - no class*		
M 12/2	IO (continued)		
T 12/3	Lab: IO Interfacing (12) KOSC 241		
W 12/4	Hardware Support for Parallelism	Computer Organization and Design (on reserve) §6.1-6.8	**LAB 12 DUE**
F 12/6	(continued)		
M 12/9	Performance Measurement and Analysis	Wikipedia article: http://en.wikipedia.org/wiki/Benchmark_(computing)	
T 12/10	Lab: Parallel Computing (13) KOSC 244		
W 12/11	Review and Catch Up		**LAB 13 DUE**
F 12/13	*No class - Reading Day*. Lab and Homework due by 4 PM		

THURSDAY, DECEMBER 19 - 9:00-11:00 AM - FINAL EXAM